Single Stage Two Phase Regulator for Mobile Microprocessor Core Voltage (ISL6223EVAL2)

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Introduction

New mobile microprocessors demand much higher current than their older counterparts. As a result, a single phase PWM converter will have difficulty to cost-effectively handle the required load current. In addition, the power management of these microprocessors dynamically change the core voltage and the core frequency to minimize the power consumption for given applications. The VID code is dynamically adjusted in these processors, which can be referred to as “VID-on-the-fly.” The ISL6223 two-phase PWM controller IC is designed for powering these new mobile microprocessors. The ISL6223EVAL2 evaluation board will demonstrate the performance of the ISL6223 for single-stage power conversion, converting directly from a battery voltage to a microprocessor core voltage. Features of the controller, such as VID-on-the-fly, are demonstrated.

Board Description

A simplified view of the ISL6223EVAL2 board is shown in Figure 1. The required components for the converter are the ones inside in the *Controller* and *Power Components* blocks. The components in the *VID Selection* and *5V Bias* blocks are auxiliary, just for the convenience of the demonstration. It is important to know the terminals, jumpers, and the switches of this evaluation board.

Terminals

Three pairs of terminals are on the board. The pair on the top edge of the board are the battery voltage input terminals, labeled as VBAT and GND. The pair labeled with VCORE and GND on the bottom edge are the core voltage output terminals. The 5V and GND pair is for the bias voltage of the controller IC. This terminal pair can be a 5V input or output, depending on whether or not the 5V on-board linear regulator is populated. Currently the linear regulator is not populated so an external 5V bias should be connected.

Jumpers

On the left edge of the board are one set of VID jumpers as well as one set of SVID jumpers. These jumpers are for setting up the VID inputs of the DC-DC converter.

Switches

In the upper left corner is the Enable (EN) switch. The EN switch enables or disables the converter depending on its position. When the switch in flipped to the left position (position 1), the converter is enabled.

Also in the upper left corner is the FLY push button. The controller will take the code either labeled with VID or SVID as its input VID code. One can switch between the two sets of VID by pushing the FLY push button. Such setting is for demonstrating the VID-on-the-fly feature. At power up, the controller always takes VID as the initial input, not SVID.

Power Good Indicator

Finally, on the top and center portion of the board is the PGOOD LED. When the core voltage is within the specified value, the LED lights up.

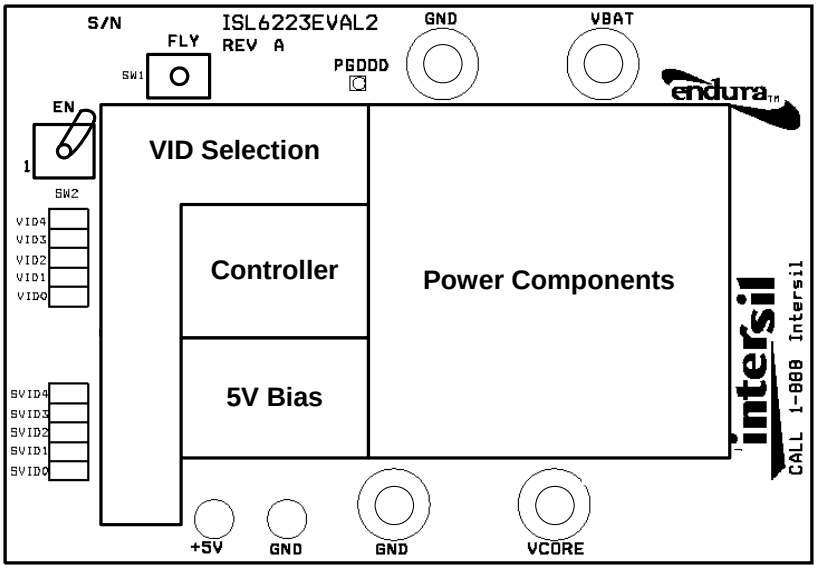


FIGURE 1. TOP VIEW OF ISL6223EVAL2 EVALUATION BOARD (ACTUAL BOARD SIZE)

Powering Up

Before powering up, connect a voltage source capable of 24V output voltage and 10A output current to the VBAT and its GND. Also connect a 5V bias voltage to the 5V and GND terminals. The 10A current is required to avoid triggering over current protection during load transient. Connect a load of up to 22A to the VCORE and GND terminals. Then the board can be applied power. No special sequencing is required for the 5V and the battery voltages. Neither is there a requirement for the initial position of the EN switch. After applying power, the converter can be enabled or disabled by flipping the EN switch.

Design Parameters

Input Voltage (VBAT):	5V to 24V
Bias Voltage (5V):	5V +/- 5%
Output Voltage (VCORE):	Set by VID
Load Current:	0A to 22A
Switching Frequency:	200kHz

Schematic and Layout

See the Appendix for the schematic, the bill-of-materials, and the layout layers.

Evaluation Measurements

The following sections show the evaluation measurements taken from this evaluation board. Refer to the schematic for the test point names used below.

Start-up Transient

Figure 2 shows the start up waveforms initiated by closing the EN switch. From top to bottom, the waveforms are PWM1, PGOOD, VCORE, and EN switch output. The EN switch output is also the gate voltage of Q18. As the EN output falls, Q18 is turned off and the ISL6223 softly starts up the output. The delay time from the falling edge of the EN signal to the rising edge of PGOOD is about 20ms. Both 5V bias and the 12V battery voltage are available before closing the EN switch in this case.

Figure 3 shows the start-up waveforms initiated by the UVLO (undervoltage lockout) of ISL6223. In a battery-powered system, the battery voltage is always available before any other voltages. Figure 3 demonstrates such a case with the 12V battery input available before the 5V bias. The EN switch is flipped to the left position, i.e. the enable position. It is shown that the PGOOD signal is asserted after the VCORE is completely within regulation range.

Load Transient Response

Figure 4 shows the transient in response to a step-up load. The input battery voltage is 12V and the output voltage is set to 1.3V nominal. The load current steps from 0A to 22A with its slew rate limited by the electronic load (Chroma 63103) at 2.5A/µs. Because of the slow slew rate of the electronic load, the initial drop of the output voltage caused the ESR and ESL of the output capacitors can not be seen here. Figure 4 does show that the inductor current reaches the full-load current in about 10µs and the approximately 50mV droop voltage at the VCORE output.

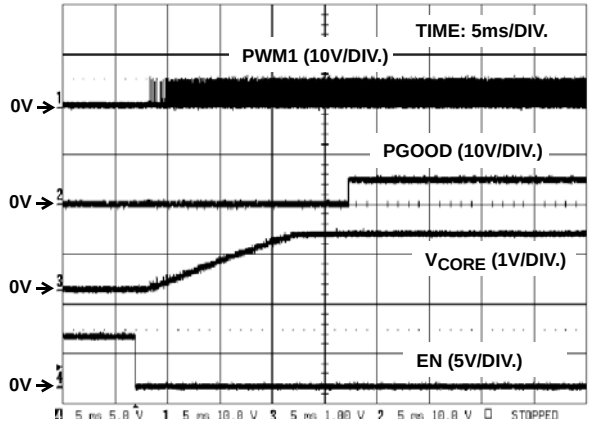


FIGURE 2. START UP INITIATED BY EN SWITCH

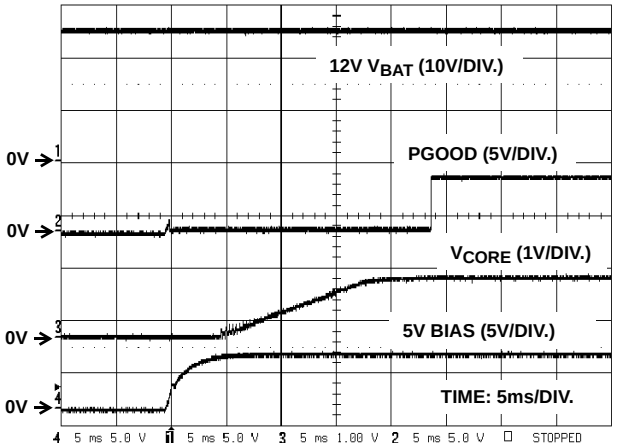


FIGURE 3. START UP INITIATED BY UVLO

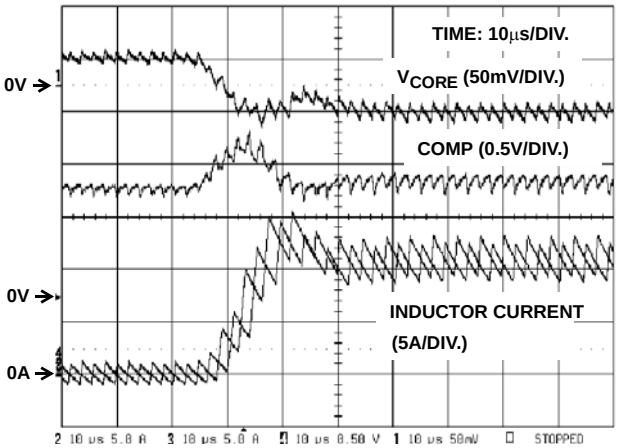


FIGURE 4. LOAD FROM 0A TO 22A TRANSIENT

Figure 5 shows the load step response from 22A to 0A. The slew rate of the load is again limited by the electronic load at 2.5A/µs. The VCORE shows a 70mV overshoot. For a single-stage conversion with large voltage step-down conversion ratio, the transient voltage for load step up and down are usually not symmetrical. This is because for such applications, the steady-state duty ratio is quite small. For the case shown here, the duty ratio is about 12% with 12V input and 1.3V output. The converter has much larger range of duty ratio (hence, much larger voltage) in response to load step up than to load step down; therefore, it usually responds faster with smaller transient voltage for load step up than for load step down. Fortunately, the power requirement for mobile microprocessor core voltage allows larger window for load step down transient (overshoot) than for load step up transient (undershoot), such as what is specified in reference [1] from AMD. The specification in reference [1] allows 150mV overshoot and only 100mV undershoot.

VID-on-the-Fly

The two sets of jumpers on the ISL6223EVAL2 board allow the demonstration of VID-on-the-fly. After power up, the FLY button can be pushed to dynamically change the VID code from one value to another, set by the VID jumpers and SVID jumpers. As mentioned earlier, at power up, the core voltage is always set by the VID jumpers first.

Figure 6 and 7 demonstrate the behavior during VID-on-the-fly. Figure 6 shows the case when the core voltage changes from 1.3V to 1.6V while Figure 7 shows the case when the core voltage changes from 1.6V to 1.3V. In both cases the core voltage is loaded with 10A current. From top to bottom, the waveforms are the DACOUT pin voltage, the core voltage, and the two inductor currents. For the step up transition shown in Figure 6, the transient finishes in less than 50µs. The total inductor current peaks at about 27A. The transition speed is determined by C14, the capacitor that is connected between the GND and the DACOUT pin. The current value for C14 is 22nF. Increasing the value of C14 will slow down the voltage transition and reduce the peak inductor current. These two figures also demonstrate how well the two inductor currents track each other during the transient and the steady-state operation.

Input Ripple Current

The input ripple current is shown in Figure 8. No filtering inductor is employed except for a pair of #18 gauge wires of 5 inches each connecting the power supply to the VBAT and GND terminals. From top to bottom are the two phase node voltages, the input current, and the input voltage. The ripple voltage caused by the pulsating current is obviously seen. The input battery voltage is 12V and the output is 1.2V with 22A load.

Input Step Response

Figure 9 shows the output VCORE in response to a step battery input change. Such large input step occurs when the battery charger is plugged into a mobile computer. Figure 9 shows the response when BVAT changes from 5V to 19V in 20µs. The output is set to 1.2V with 10A load current. A 40mV perturbation is observed at the VCORE output. Figure 10 shows the step down transition for the input voltage with the same output and load condition. The slew rate of the input voltage is dependent on the discharging current of the input capacitors. A transient voltage of 20mV is observed in this case.

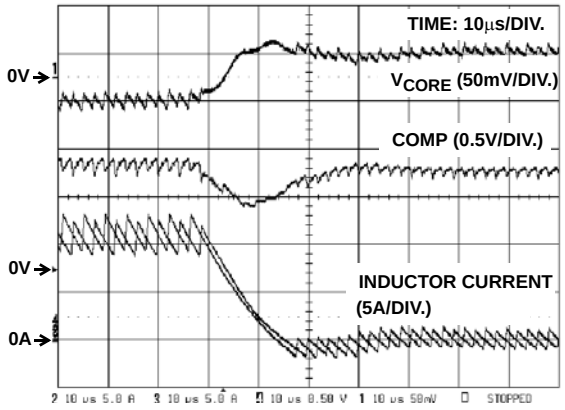


FIGURE 5. LOAD FROM 22A TO 0A TRANSIENT)

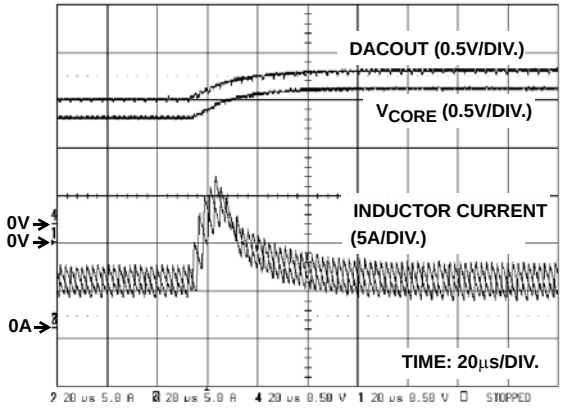


FIGURE 6. VID-ON-THE-FLY, CHANGING FROM 1.3V TO 1.6V

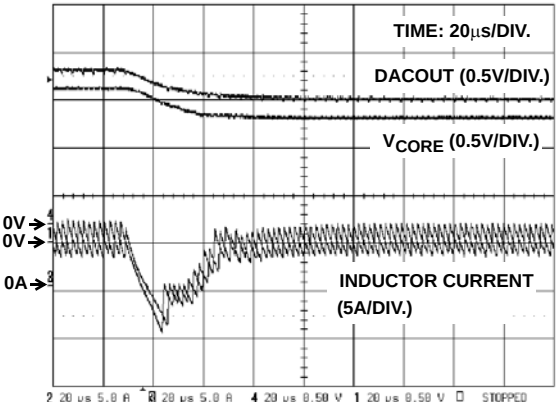


FIGURE 7. VID-ON-THE-FLY, CHANGING FROM 1.6V TO 1.3V

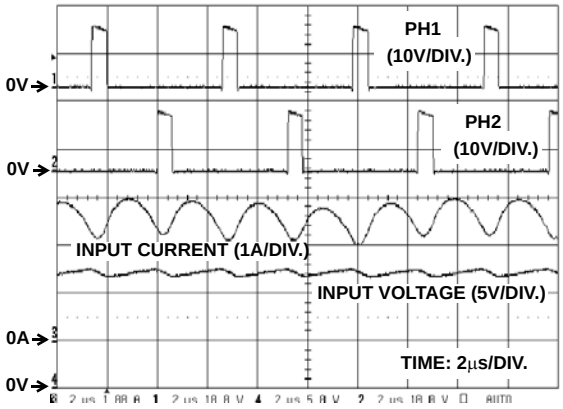


FIGURE 8. INPUT RIPPLE CURRENT

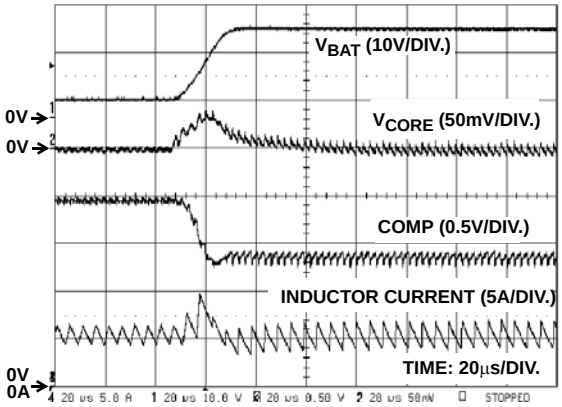


FIGURE 9. INPUT VOLTAGE STEP UP TRANSIENT RESPONSE

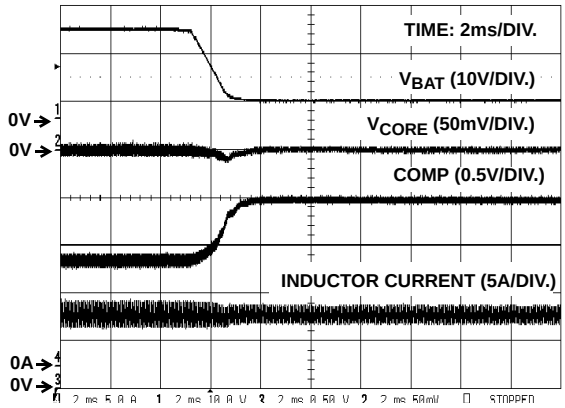


FIGURE 10. INPUT VOLTAGE STEP DOWN TRANSIENT

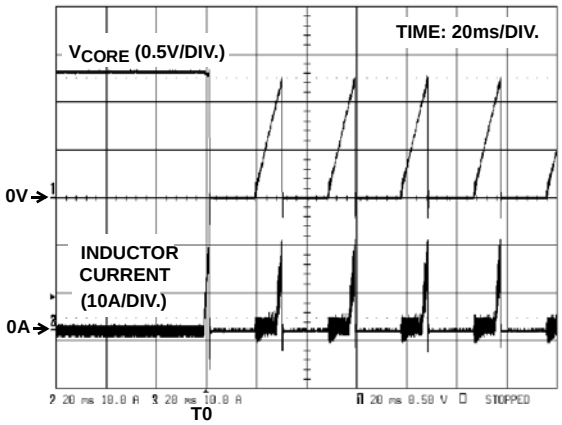


FIGURE 11. OUTPUT OVERCURRENT PROTECTION

Output Overcurrent Protection

Figure 11 demonstrates the converter's reaction to an output overcurrent event. At time T0, the converter is loaded with a 40A current from the Chroma 63103 electronic load. The converter quickly ramps up the inductor current, hits the 35A overcurrent protection threshold, and then triggers the over current protection function. The converter shuts down. After a waiting period of approximately 20ms, the converter tries to start up again. When the output voltage reaches 1V, the electronic load is enabled again with the 40A load, triggering another overcurrent event. If the over current persists, the converter operates in the hiccup mode. The average heat generated in the hiccup mode is less than the heat generated under a full-load condition so the converter is protected and operates safely.

Droop Voltage vs Load Current

The purpose of the droop voltage is to enlarge the allowed transient voltage window so as to reduce the number of the output capacitors. By adjusting the values of the R_{ISEN} (R2 and R10) and the feedback resistor (R6), one can design the droop slope to a different value. Of course, when adjusting these resistor values, the overcurrent protection tripping level is changed and the loop compensation components need adjustment as well. Figure 12 shows the measured droop voltage vs. load current at three different input voltages with the resistor values given in the bill-of-materials. The nominal voltage is set to 1.3V for this case. The droop voltage is quite independent of the input voltage. A 45mV droop is measured as the load moves from 0A to 22A.

Efficiency

Figure 13 shows the measured efficiency at various input voltages and load currents. One top MOSFET and two bottom MOSFETs are employed in the evaluation board, all ISL9N308. The measurements were made at room temperature with natural convection cooling only.

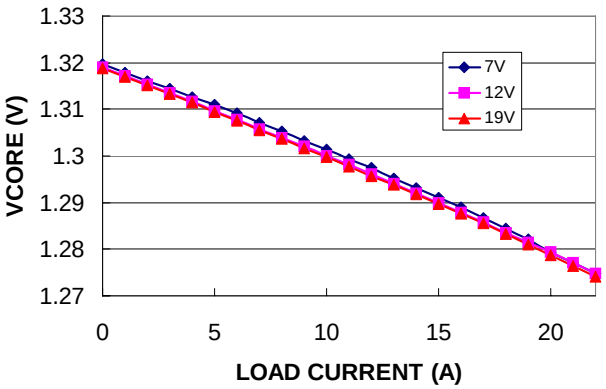


FIGURE 12. CORE VOLTAGE vs LOAD CURRENT

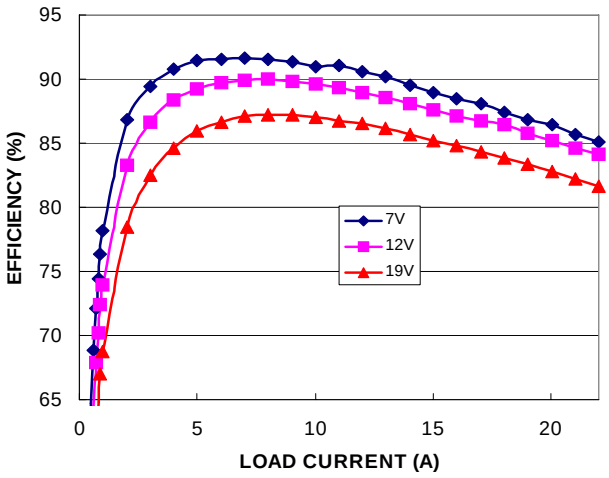


FIGURE 13. EFFICIENCY MEASUREMENT.

Conclusion

The ISL6223EVAL2 is designed to provide a convenient platform to evaluate the performance of ISL6223 for single-stage power conversion for mobile computing applications. This evaluation board demonstrates that using ISL6223 results in a high efficiency, cost-effective solution to meet all the power requirements posed by the mobile microprocessor core.

References

For Intersil documents available on the internet, see web site www.intersil.com

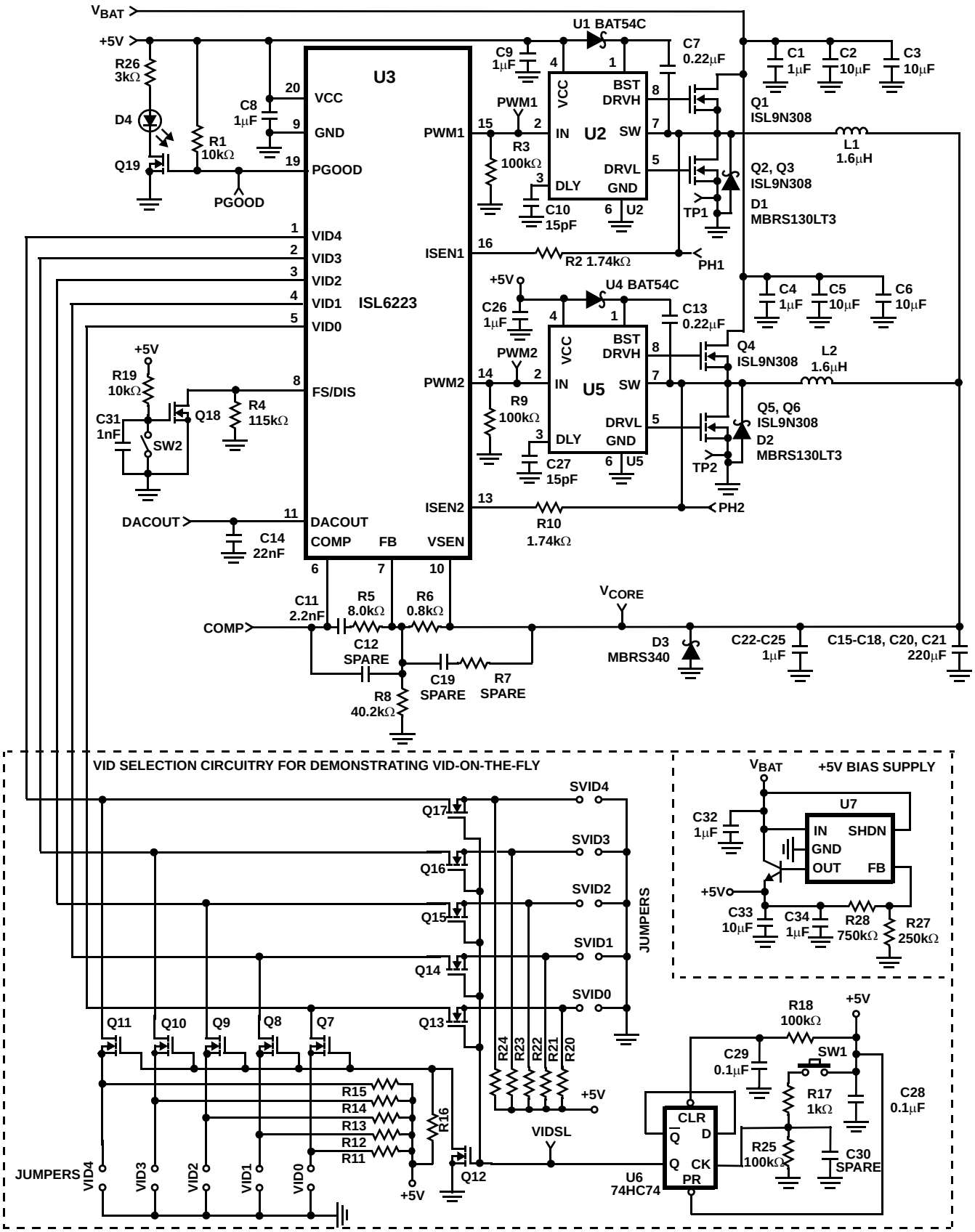
Intersil Technical Support 1-888-INTERSIL

[1] AMD, *Mobile AMD Athlon™ and Mobile AMD Duron™ Processor 24W Power Module Design Guide,* 10/18/00.

[2] *ISL6223 Data Sheet*, Intersil Corporation, Power Management Products Division.

Appendix

Schematic

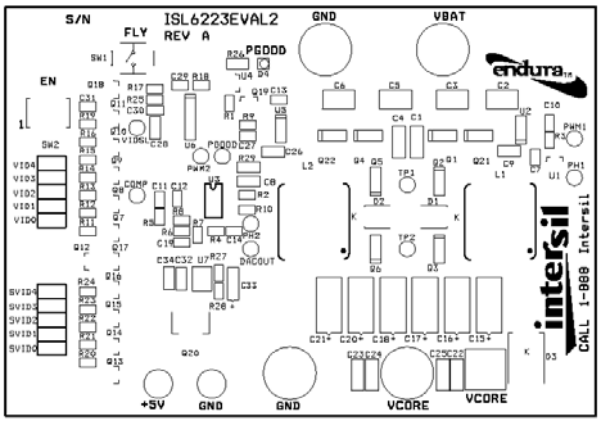


Bill of Materials

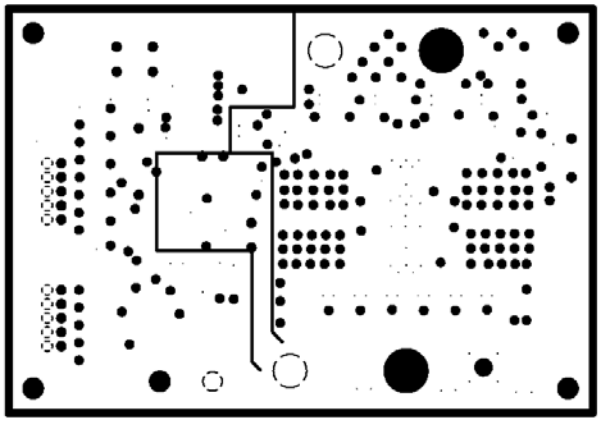
QTY	REFERENCE	DESCRIPTION	PCB FOOTPRINT	PART#	VENDOR	COMMENTS
2	C1, C4	1µF, Y5V, 25V	SM/C_1206	PCC1903CT-ND	Digikey	
4	C2, C3, C5, C6	10µF, Y5V, 35V	SM/C_1210	GMK325F106ZH	Taiyo Yuden	
2	C7, C13	0.22µF, Y5V, 16V	SM/C_0603	PCC1790CT-ND	Digikey	
9	C8, C9, C22, C23, C24, C25, C26, C32, C34	1µF, Y5V, 16V	SM/C_0805	PCC1849CT-ND	Digikey	C32 SPARE
2	C10, C27	15pF, NPO, 50V	SM/C_0603	PCC150ACVCT-ND	Digikey	
1	C11	2.2nF, X7R, 50V	SM/C_0603	PCC222BCVCT-ND	Digikey	
1	C12	SPARE	SM/C_0603			SPARE
1	C14	22nF, X7R, 25V	SM/C_0603	PCC223BVCT-ND	Digikey	
6	C15, C16, C17, C18, C20, C21	220uF, 2.5V, UE SERIES SP CAP		EEFUE0E221R	Panasonic	C21 SPARE
2	C19, C30	SPARE	SM/C_0603			SPARE
1	C28	0.1µF, Y5V, 16V	SM/C_0805	PCC1849CT-ND	Digikey	
1	C29	0.1µF, Y5V, 16V	SM/C_0603	PCC1788CT-ND	Digikey	
1	C31	1nF, X7R, 50V	SM/C_0603	PCC1772CT-ND	Digikey	
1	C33	10µF, 10V, TANTALUM		TPSA106*010#1800	AVX	
2	D2, D1	1A, 30V, Schottky Diode	SMB	MBRS130LT3	On Semi	
1	D3	3A, 40V, Schottky Diode	SMC	MBRS340LT3	On Semi	
1	D4	LED		L63311CT-ND	Digikey	
4	JP1, JP2, JP3, JP4	Banana Binding Post	BINDING/POST		Various	
10	JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14	2-Pin Jumper		S9001-ND	Digikey	
2	L1, L2	1.6µH Inductor		ETQP6F1R6S	Panasonic	
8	Q1, Q2, Q3, Q4, Q5, Q6, Q21, Q22	Power MOSFET	SO-8	ISL9N308ASK8T	Intersil	Q21, Q22 SPARE
13	Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19	MOSFET	SM/SOT23_GSD	2N7002	Fairchild	
1	Q20	NPN Transistor	SOT-223	PZT2222AT1	Motorolla	SPARE
1	R1	10K, 5% Res	SM/R_0603		Various	
2	R10, R2	1.74K, 1%	SM/R_0603		Various	
2	R3, R9	100K, 5% Resistor	SM/R_0603		Various	
1	R4	115K, 1%	SM/R_0603		Various	
1	R5	8K, 1% Res	SM/R_0603		Various	
1	R6	0.8K, 1% Res	SM/R_0603		Various	
1	R7	SPARE	SM/R_0603		Various	SPARE
1	R8	40.2K, 1% Res	SM/R_0603		Various	
11	R11, R12, R13, R14, R15, R19, R20, R21, R22, R23, R24	10K, 5% Res	SM/R_0603		Various	
1	R16	3.3K, 5%	SM/R_0603		Various	
1	R17	1K, 5% Res	SM/R_0603		Various	
2	R25, R18	100K, 5% Res	SM/R_0603		Various	
1	R26	3K, 5% Res	SM/R_0805		Various	
1	R27	250kΩ, 1% Res	SM/R_0603		Various	SPARE
1	R28	750K, 1% Res	SM/R_0603		Various	SPARE
1	R29	0Ω Jumper	SM/R_0603		Various	
1	SW1	SW Pushbutton		SW_P8007S-ND	Digikey	
1	SW2	SW MAG-SPST		SW-GT12MSCKE	Digikey	
1	VCORE	Probe Socket			Tektronics	
2	TP21, TP22	Connector			Digikey	
2	U4, U1	Schottky Diode	SOT-23	BAT54C	Fairchild	
2	U5, U2	Gate Driver	SOIC	ADP3412	ADI	
1	U3	Two-Phase Controller	SSOP	ISL6223	Intersil	
1	U6	Dual D FlipFlop	SOIC	74AHC74/SO	TI	
1	U7	Voltage regulator	SOT23-5	MAX1616	Maxim	SPARE
10	Test Points	Test Point	TP	5002K-ND	Digikey	

Layout Drawings

SILKSCREEN TOP



GND-INTERNAL 1



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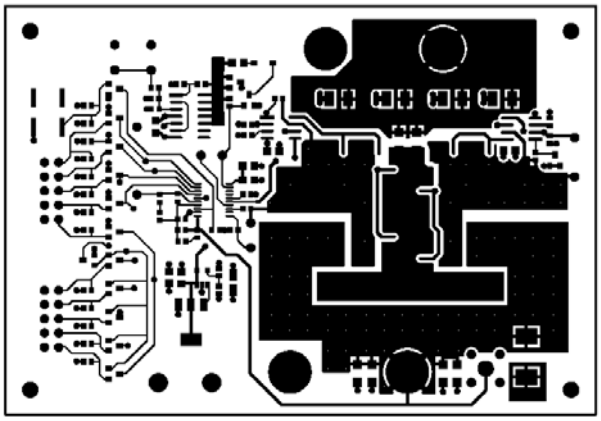

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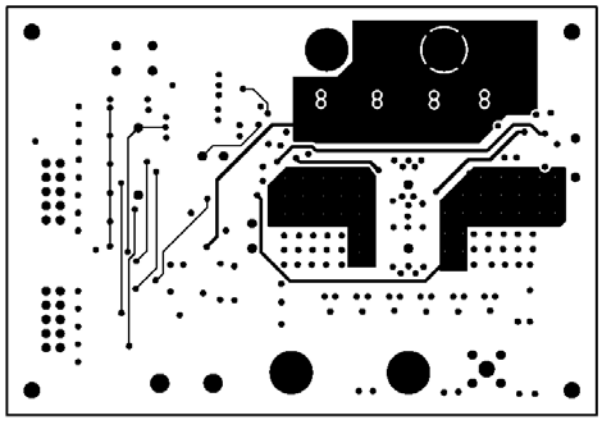
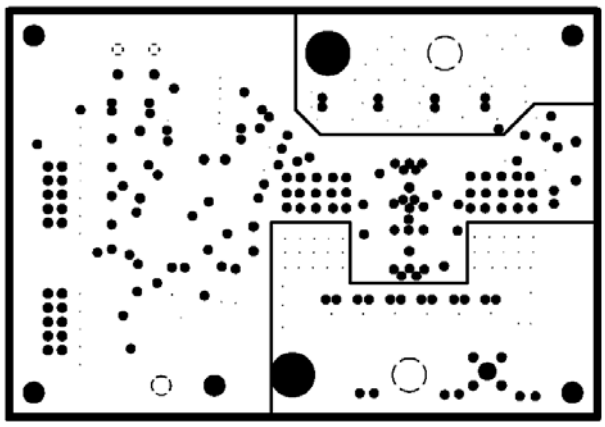


POWER-INTERNAL2



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